Abstract of the Disclosure:

The invention relates to an interface with parallel transfer channels for transmission of a number of parallel data signals and, possibly, command signals between associated outer connections and associated circuit points in an electronic assembly. A synchronization signal connection carries a synchronization signal indicating the time base for the parallel-transmitted signals. Selected examples of the transfer channels each contain an individually controllable delay device for setting a time delay for a signal transmission in the relevant transfer channel. Furthermore, a control device is provided in order to sense, in each selected transfer channel, the actual value of the relative phase of the data signal with respect to the associated, accompanying synchronization signal, and to control each of the delay devices as a function of the respectively sensed actual value, in the sense of matching the actual value to a predetermined, common nominal value.

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